REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendments and the following remarks.

Allowable Subject Matter

As a preliminary matter, Applicants appreciate the indication of allowable subject matter in claims 21-27, 38, 39, 43 and 45 of the present application.

Summary of the Response

By the foregoing amendments, claims 1, 4, 8, 12, 20, 28-29, 40-41, 44 and 47 have been amended. Thus, claims 1-47 are currently pending in the application and subject to examination.

In the Office Action mailed on September 3, 2004, claims 1-20, 28-37, 40-42, 44, 46 and 47 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,515,906 to Tedrow, et al. To the extent that the rejections remain applicable to the claims currently pending, the Applicants hereby traverse the rejections, as follows.

Independent Claims 1, 8 and 20 Recite Patentable Subject Matter

Regarding claims 1, 8 and 20, Applicants respectfully submit that Tedrow, et al. does not teach or suggest all of the features recited in these claims. For example, Tedrow, et al. fails to teach or suggest at least the features of the present invention of a "second digit line connected to the plurality of nonvolatile memory cells including only non-selected nonvolatile memory cells which are in a second memory block and are not subject to the reading [or access]," as recited in amended claims 1 and 20, and of a "second global digit line connected to a second local digital line [serving as a reference

bit line] to which the plurality of nonvolatile memory cells including only non-selected nonvolatile memory cells which are adjacent to the first global digital line and in a second memory block of the memory blocks and are not subject to the reading," as recited in amended claim 8 of the present application.

These features are illustrated, for example, in Figure 2 of the present application. As shown in Figure 2, control signal SECYm and Sm and word line WLm are activated and nonvolatile transistor MCm is selected in sector SECm. A local bit line LBLm is connected to a global bit line GBLm by a switch-select switch SSm, to read out data from the nonvolatile transistor MCm. The nonvolatile transistor MCn in sector SECn is not selected, but a switch SSn is conducted by a circuit 10 to connect a local bit line LBLn to a global bit line GBLn. The local bit line LBLn to which the non-selected nonvolatile transistor MCn is connected is a reference bit line. Thus, a parasitic parameter parasitizing a digit line is added to the digit line for data read-out and also to the digit line for reference. This makes it possible to enhance the characteristics of data reading.

By contrast, in Tedrow, et al., the bit line serving as a reference is not connected to a local bit line in the memory block (ODD or EVEN), even through transistors (715B-745B or 715A-745A) and another bit line with which data is read out. *See, e.g.* Figures 7A and 7B.

For at least these reasons, Applicants submit that claims 1, 8 and 20, as amended, are allowable over the cited prior art.

Independent Claim 29 Recites Patentable Subject Matter

Regarding claim 29, Applicants submit that nothing in Tedrow, et al. discloses or suggests at least the features of "a first loading portion connected to the first data line; and a second loading portion having a structure equivalent to that of the first loading portion, connected to the second data line and for supplying a reference current to a current flowing through the first data line based on the memory cell information, wherein the memory cell information is read out with the first and second data lines as a pair," as recited in amended claim 29 of the present application. As illustrated, for example, in Figure 1, the first and second loading portions are connected to each data line provided for every predetermined number of digit lines.

By contrast, in Tedrow, et al., a reference cell array is disposed adjacent to a memory cell block in a memory cell array. Each global bit line is provided with a reference cell. *See* Figure 5.

The present invention, therefore, needs only a few reference cells as compared with the disclosure of Tedrow, et al. This may reduce variations between reference cells resulting from a manufacturing process and may further lead to shortening the time needed for adjusting the characteristics of current in each reference cell.

For at least these reasons, Applicants submit that claim 29, as amended, is allowable over the cited prior art.

Independent Claims 41 and 44 Recite Patentable Subject Matter

Regarding claims 41 and 44, Applicants submit that nothing in Tedrow, et al. discloses or suggests at least the features of a "connection changing portion for holding

a predetermined connecting relation to the first and second data lines to the current load portion by changing a connection between the data lines and the current load portion," as recited in amended claim 41, and of a "first data line to which the selected nonvolatile memory cell which is subject to reading of memory cell information is connected through the digit line and through which a current based on the memory cell information flows; a second data line through which a reference current flows; and a current comparing portion to which the first and second data lines are connected and which compares a current based on the memory cell information with the reference current, wherein the current comparing portion includes a current load portion for supplying a current equivalent to the reference current to the first and second data lines," as recited in amended claim 44 of the present application.

Tedrow, et al. only discloses, as shown in Figure 5, that the input to DRAIN BIAS & SENSE AMP varies depending on a selected memory block. *See* column 6, lines 32-35. The data reading/reference bit line is inverted by position/negative input according to the selected memory block.

By contrast, referring to claim 41, the current invention includes a connection changing portion that can hold a predetermined connecting relation of the digit line for data reading/reference to a current loading portion. It is therefore possible to correctly read data even by use of a differential amplifier provided with a reference terminal fixed therein, as shown in Figures 15 and 16.

Furthermore, referring to claim 44, correct reading can be made even where the data-reading/reference digit line is connected to any terminal of the current loading portion, as shown for example in Figures 15 and 17.

For at least these reasons, Applicants submit that claims 41 and 44, as amended, are allowable over the cited prior art.

Dependent Claims 4 and 12 Recite Patentable Subject Matter

Applicants respectfully submit that as claims 1 and 8 are allowable, claims 4 and 12, which respectively depend from allowable claims 1 and 8, are likewise allowable over the cited prior art.

In addition, Applicants submit that nothing in Tedrow, et al. teaches or suggests at least the features of "a positional relationship of the first digit line and the second digit line is inverted by each of the memory block," as recited in amended claim 4, and of a "positional relationship of the first local digit line and the second local digit line . . . inverted every memory block," as recited in amended claim 12 of the present application.

In describing Figure 5, Tedrow, et al. indicates that "the state definition of even-numbered blocks will be inverted relative to odd-numbered blocks" because "the reference cell is coupled to either the positive or negative input of the sense amplifier." See, e.g., column 6, lines 32-37.

By contrast, in the present application, the first and second digit lines are provided to have an inverted positional relation in a layout according to each memory block. Figure 3, for example, shows that the positions of the global bit lines (GBL0 and GBL1, GBL2 and GBL3) are interchanged between the sectors (SEC0 and SEC1). Thus, in contrast to the disclosure in Tedrow, et al., an object of the present invention is to balance the parasitic parameter between a pair of digit lines.

For at least these reasons, Applicants submit that claims 4 and 12, as amended, are allowable over the cited prior art.

Dependent Claim 30 Recites Patentable Subject Matter

Applicants respectfully submit that as claim 29 is allowable, claim 30, which depends from allowable claim 29, is likewise allowable over the cited prior art.

In addition, Applicants submit that nothing in Tedrow, et al. teaches or suggests at least the feature of a "first and second loading portions [that] have a load equivalent to a load existing on a path leading from the nonvolatile memory cell to the first and second loading portions," as recited in claim 30 of the present application. As shown in Figure 10, for example, the first or second loading portion to be connected to the reference bit line have the same load, which can place the data reading bit line and the reference bit line into a balanced loading state.

By contrast in Tedrow, et al., the transistor (715A to 745A or 715B to 745B) is conducted by the bit line for data reading, whereas it is not conducted by the bit line to be connected to the reference cell, in which a load varies between the memory cell and a DRAIN BIAS and SENSE AMP. *See* Figures 5, 7A and 7B.

For at least these reasons, Applicants submit that claim 30 is allowable over the cited prior art.

Dependent Claim 32 Recites Patentable Subject Matter

Applicants respectfully submit that as claim 29 is allowable, claim 32, which depends from allowable claim 29, is likewise allowable over the cited prior art.

In addition, Applicants submit that nothing in Tedrow, et al. teaches or suggests at least the feature of a "regulating portion containing a third reference cell equivalent to the nonvolatile memory cell, for generating a reference current with respect to a current based on the memory cell information and outputting a regulation voltage corresponding to the reference current, wherein the first and second loading portions have first and second load portions in which a current value is controlled by the regulation voltage," as recited in claim 32. As shown in Figure 12, for example, the reference cell has only to be provided one for a pair of digit lines. This makes it possible to reduce manufacturing variations between the reference cells and to shorten the time needed for adjusting the characteristics of current in each reference cell.

By contrast in Tedrow, et al., the reference array is arranged adjacent to the memory cell block in the memory cell array. *See* Figure 5. The reference cell is provided for each global bit line.

For at least these reasons, Applicants submit that claim 32 is allowable over the cited prior art.

Dependent Claims 2-3, 5-7, 9-11, 13-19, 23, 25, 28, 31, 33-34, 35-37, 40, 42 and 46-47 Recite Patentable Subject Matter

Applicants respectfully submit that as claims 1, 8, 20, 29 and 41 are allowable, claims 2-3, 5-7, 9-11, 13-19, 23, 25, 28, 31, 33-34, 35-37, 40, 42 and 46-47, each of which depends from allowable claims 1, 8, 20, 29 or 41, are likewise allowable over the cited prior art.

Dependent Claims 21-22, 24, 26-27, 38-39, 43 and 45 Recite Patentable Subject Matter

As the Examiner indicated in the Office Action, claims 21-22, 24, 26-27, 38-39, 43 and 45 are allowable.

Conclusion

For all of the above reasons, it is respectfully submitted that the claims now pending patentably distinguish the present invention from the cited references. Accordingly, reconsideration and withdrawal of the outstanding rejections and an issuance of a Notice of Allowance are earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is encouraged to telephone the undersigned representative at the number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300, referring to client-matter number 024016-00025.

Respectfully submitted,

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Enclosure: Petition for Extension of Time (one month)

TECH/276515.1